I CLAIM:

1. A method of stabilizing two current loops within a circuit comprising the steps of:

providing a main current loop for supplying current to a load;

providing a sensing loop for monitoring the current to the load;

an error amplifier coupled to the output of the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and

providing capacitance to each loop whereby stability is independently maintained for each loop within selected operational criteria.

2. A method according to claim 1 wherein the coupling step further comprises coupling the output of the error amplifier to the gate of a transistor and coupling the output of the sensing loop to the source of the transistor.

3. A method according to claim 1 wherein the output of the main loop comprises a low impedance node.

4. A method according to claim 1 wherein the output of the main loop comprises a high impedance node.

5. A circuit stabilization method according to claim 1 wherein the main loop further comprises a low dropout regulator (LDO).

6. A circuit having a low capacitive load and comprising two stable current loop sub circuits further comprising:

a main current loop for supplying current to the load, the main current loop having a first compensation capacitor for maintaining stability within a pre-selected operational range;

a sensing loop for monitoring the current to the load, the sensing loop having a second compensation capacitor for maintaining stability within a pre-selected operational range; and

a transistor for coupling the output of the main current loop and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor.

7. A circuit according to claim 6 wherein the transistor further comprises a MOSFET.

8. A circuit according to claim 6 wherein the transistor further comprises a bipolar transistor.

9. A circuit according to claim 6 wherein the output of the error amplifier is coupled to the gate of the transistor and the output of the sensing loop is coupled to the source of the transistor and to the second compensation capacitor.

10. A circuit according to claim 6 wherein the main loop further comprises an error amplifier and wherein the output of the main loop comprises a low impedance node of the error amplifier.

11. A circuit according to claim 6 wherein the main loop further comprises an error amplifier and wherein the output of the main loop comprises a high impedance node of the error amplifier.

12. A circuit according to claim 6 wherein the main loop further comprises a low dropout regulator (LDO).

13. A circuit according to claim 6 wherein the load capacitance of the circuit is on the order of approximately 1uF.

14. A method of stabilization of a circuit having a capacitive load on the order of approximately 1uF and having two current loop sub circuits comprising the steps of:

providing a main current loop for supplying current to the load, the main current loop having a first compensation capacitance for maintaining stability within a pre-selected operational range;

providing sensing loop for monitoring the current to the load, the sensing loop having a second compensation capacitance for maintaining stability within a pre-selected operational range; and

coupling the output of the main current loop and the output of the sensing loop such that the first compensation capacitance is isolated from the second compensation capacitance.

15. The method according to claim 14 wherein the output of the main current loop is coupled to the gate of a transistor and the output of the sensing loop is coupled to the source of the transistor.

16. The method according to claim 14 wherein the output of the main loop further comprises an error amplifier and wherein the output of the main loop comprises a low impedance node of the error amplifier.

17. The method according to claim 14 wherein the main loop further comprises an error amplifier and wherein the output of the main loop comprises a high impedance node of the error amplifier.

18. The method according to claim 14 used in a low dropout regulator (LDO).